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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application	Applicant(s)	
	09/862,471	KAWAGUCHI, MITSUHARU	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004 and 11 October 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3 and 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 have been examined.

Papers Received

2. Receipt is acknowledged of priority, two information disclosure statement, formal drawings, and change of address papers submitted, where the papers have been placed of record in the file.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statement (IDS) submitted on 23 May 2001 is in compliance with the provisions of 37 CFR 1.97 and the examiner has considered the references to the extent possible without an understanding of the Japanese language.

Drawings

5. The drawings are objected to because figures 1-4 do not provide enough detail for a proper understanding of the invention. 37 CFR 1.83(a) states that conventional features, where the detailed description is not essential for proper understanding of the invention, require a labeled graphic or rectangular box for example. It is very difficult to ascertain what the structure of the system comprising the invention is without some sort of descriptive labels in addition to the reference numbers of these figures. The Examiner requests that these figures be presented in a more self-descriptive manner. A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the subject matter described in claims 6-10 regarding groups of instructions is not disclosed in the detailed description. The claims read on the disclosed description if one formulates their own groups through deduction, however, the claimed subject matter must be more adequately described since multiple groups of instructions in the detailed description can be interpreted to read on the claims and thus the description is not aimed at the claimed subject matter.

8. The disclosure is objected to because of the following informalities: One of ordinary skill in the art would be able to make and use the claims in light of themselves so there is currently no enablement issue.

9. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: An Instruction Buffer and Method of Controlling the Buffer where Entries of the Buffer are Issued Based on an Associated Lowest Entry Number.

Appropriate correction is required.

Claim Objections

10. Claim 1 is objected to because of the following informalities: the claim uses the phrases "low entry number" and "high entry number". The bounds of the terms "low" and "high" are indefinite. There is no frame of reference or definition of these bounds. The examiner is taking the claim to mean "lower entry number" and "higher entry number" so that the two numbers are relative to each other as makes sense in the context of the claims.

11. Claims 6 and 7 are objected to because of the following informalities: the claims use the phrase "highest in order." It is unclear what this means. In light of the specification, it could refer to the instruction with the highest entry number, which would be contrary to the teaching of the specification where the instruction with the lowest entry number is executed first. The examiner is taking the phrase to mean "highest in priority" based on the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 5 and 7-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claim 5 recites the limitations "the instruction" in line 3 and "the other instructions" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. It is unknown which instruction is "the instruction" in the claim since an entire sequence has been defined. The examiner is taking the limitation to instead read "an instruction" so that anyone of the sequence may be selected. Also, it is unclear what "the other instructions" are since they have not been defined. The examiner is taking the claim to mean "other instructions" so that the term is introduced while not further limiting the scope of the claim and being in accordance with the specification.

15. Claim 7 recites the limitations "one of said fourth group of instructions" in line 8 and "none of said fourth group of instructions" in line 10. There is insufficient antecedent basis for this limitation in the claim. There has been only one fourth group of instructions defined and the claim language reads where a group of this fourth group is singled out. The examiner is taking the limitations of the claim to read "one instruction of said fourth group of instructions" and "none of the instructions of said fourth group of instructions" so that the claim refers to the instructions in the group as being selected and not the group itself.

16. Claim 8 recites the limitation "one of preselected two instructions" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim. There has not been two preselected instructions defined as of yet in the claims. Since this is the

introduction of the two instructions, the examiner is taking the claim to read "one of a preselected two instructions."

17. Claim 8 recites the limitation "the other instruction" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. It is unclear what the other instruction is. The language could lend itself to any other instruction to be executed. The examiner is taking the claim to mean "the other of the preselected two instructions" as implied by the claim and supported in the specification.

Claim Rejections - 35 USC § 102

18. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

19. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Rupley (6,157,998).

20. In regard to claim 1, Rupley discloses an instruction buffer comprising:

a. a sequence of instructions arranged in an order determined beforehand; and a first buffer including entries arranged in a preselected order for storing said sequence of instructions; Column 6, lines 28-31 show that a group, or sequence, of instructions are stored in an instruction buffer in program order (a preselected

order). Figures 2-10 show this buffer (element 20) and that is has separate entries for storing the instructions.

b. wherein any one of said sequence of instructions stored in any one of the entries designated by a low entry number is prior, in order, to another instruction stored in another entry designated by a high entry number. Figures 4-10 illustrate a progression of the sequence of instructions through the buffer. The figures show that each buffer entry is designated by an entry number ranging from 0 to 7. The progression given in figures 4-5 show specifically that an instruction with a lower entry number (0) is dispatched from the instruction buffer and is thus prior in order to an instruction with a higher entry number such as the instruction at entry 7.

21. In regard to claim 2, Rupley discloses the instruction buffer as claimed in claim 1, wherein the entries each show whether or not the instruction stored therein is ready to be issued. Column 7, lines 59-67 show that the buffer is first-in-first-out (FIFO) in nature and after dispatch, or issue, of an instruction each instruction in the buffer decrements down into an entry with a lower entry number. Thus, as shown in figures 4-5, the instruction at entry 0 is ready to be issued. This is shown by the entries based on the entry number and if it is 0 or not.

22. In regard to claim 3, Rupley discloses the instruction buffer as claimed in claim 2, wherein the instruction is first issued from, among the entries whose instructions are ready to be issued, the entry having a lowest entry number. As shown above, the instruction first issued from is at entry 0 and thus at the entry with the lowest number.

23. In regard to claim 4, Rupley discloses the instruction buffer as claimed in claim 3, wherein the entries storing the instructions are lower in entry number than the entries storing no instructions. Figure 5-7 show that once the instructions have progressed enough, there are entries at a higher entry number with no instructions compared to the entries at lower entry number with instructions.

24. In regard to claim 5, Rupley discloses the instruction buffer as claimed in claim 4, further comprising a second buffer including other entries for storing instructions, wherein an instruction stored in any one of said other entries earlier than other instructions is issued earlier than said other instructions. Figures 2-10 show that there is a second buffer 28a as well as a third and fourth buffer, 28b and 28c respectively. Column 3, lines 34-52 illustrate that these buffers include age bits for specifying what instructions in the buffers are earlier than the other instructions in the buffers. Column 7, lines 24-27 further shows this. The progression given in figures 4-7 show that instruction BC_0 is stored in buffer 28a earlier than instruction BC_1 is stored in buffer 28c. These figures will also show that the BC_0 instruction is also issued (removed from the instruction buffer and placed in the completion buffer) before the other instruction.

25. In regard to claim 6, Rupley discloses a method of controlling a buffer queue, comprising the steps of:

a. generating a first group of instructions in an order determined beforehand; Figure 4 shows a buffer 20 for storing a group of 8 instructions. Column 6, lines 28-31 show that the instructions stored in the instruction buffer are stored in program order (a preselected order).

b. generating a second group of instructions belonging to said first group of instructions and capable of being executed; The instructions ADD and BC_0 in entries 0 and 1 of the instruction buffer of figure 4 are a second group of instructions belonging to the first group (all 8 instructions) and capable of being executed (as shown in their dispatch in figures 5-10).

c. and executing one of said second group of instructions highest in priority. Figures 4-5 shows that the instruction at entry 0 is the first in order and is dispatched to execution units and placed in the completion unit 24. Column 4, lines 25-34 show that when an instruction is dispatched for execution, it is placed in the completion buffer at the same time.

26. In regard to claim 7, Rupley discloses the method as claimed in claim 6, further comprising the steps of:

a. generating a third group of instructions included in said first group of instructions; The instructions MUL and BC_2 of entries 4 and 5 are a third group of instructions included in the first group of all 8 instructions.

b. and generating a fourth group of instructions included in said first group of instructions and not dependent on said third group of instructions; The instructions SUB and BC_1 of entries 2 and 3 are a fourth group of instructions included in the first group of instructions and that are not dependent on the fourth group. Column 7, lines 35-39 show that instructions before BC_0 do not directly depend on the outcome of the branch. The same holds true for each branch and

so the instructions of the fourth group are not dependent on the instructions, and specifically the branch (BC_2), of the third group since they are preceding in order.

c. wherein when one of said fourth group of instructions highest in priority does not belong to said second group of instructions, none of said fourth group of instructions is executed. The instruction of the fourth group that is highest in priority is the SUB instruction since it has a lower entry number and is closer to the front of the FIFO buffer. This instruction is not a part of the second group, which consists of the instructions in entries 0 and 1. A scenario is shown in figure 4 where when this SUB instruction from the fourth group of instruction highest in priority, which does not belong to the second group of instructions, none of the instructions of the fourth group are executed.

27. In regard to claim 8, Rupley discloses the method as claimed in claim 7, wherein one of a preselected two instructions belonging to said third group or said fourth group is not executable until the other instruction is executed. The two instructions of group four (BC_1 and MUL) are two preselected instructions. The progression from figures 5-6 shows that the SUB instruction is executed and placed in the completion unit before the BC_1 instruction is executed since it remains in the instruction buffer. Then in figure 7 it is shown that the BC_1 instruction is executed after the SUB instruction.

28. In regard to claim 9, Rupley discloses the method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group. Figure 7 shows the case when group four is being executed and BC_1 has been correctly predicted (column 9, lines 35-37) so the

instructions of the instruction buffer will continue to be executed. The examples given after figure 7 do not illustrate this. Figures 9-10 give examples of branch mispredictions (column 9, lines 41-48) that yield the flushing of the instruction buffer. Figure 7, for example, shows that groups two and four are executed simultaneously since they are in the completion buffer at the same time. One of ordinary skill in the art would recognize that since the branch was correctly predicted in this figure and the instruction buffer was not flushed, that the instructions of group three would next be executed and in parallel with the instructions of group 4 just has been shown to be the case with the preceding groups of instructions with correctly predicted branches.

29. In regard to claim 10, Rupley discloses the method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group are operation instructions and memory access instructions respectively. Figure 4 shows that the third group consists of MUL (multiply) and BC_2 (conditional branch) instructions. Since the conditional branch must resolve a condition it performs an operation and is an operation instruction just as the multiply instruction is. The fourth group of instructions consists of SUB (subtract) and BC_1 (conditional branch) instructions. It is inherent that a subtract instruction accesses either a main memory (or cache memory) or a register, which is a type of memory, in order to do the calculation. Therefore this instruction is a memory access instruction. A conditional branch instruction also must access some sort of memory to evaluate the condition, whether this memory is main memory, a general-purpose register, or a flag or status register.

Conclusion

30. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

31. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents have been cited to further show the art with respect to instruction buffering in general.

US Pat No 6,625,746 to Moore discloses an instruction buffer where age (an entry number) of the instruction is a consideration for issuance.

US Pat No 5,903,918 to Bauman teaches a system that issues instructions from an instruction buffer based on the ages of the instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7305. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

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March 30, 2004

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